REMARKS

Claims 1- 20 are pending in the instant patent application. Claims 8 - 9 are amended herein. No new matter has been added as a result of the amendments.

CLAIM REJECTIONS

35 U.S.C. §102 Rejections

Claim 8 is rejected under 35 U.S.C. 102(e), as being anticipated by Jaussi et al., U.S. Patent No. 6,737,909 (hereinafter Jaussi). Applicants have reviewed the cited portions of the reference, and submit that the embodiment of the present invention as recited in Claim 8 is neither anticipated nor rendered obvious by the cited portions of Jaussi.

Examiner is respectfully directed to amended independent Claim 8, which recites that an embodiment of the present invention is directed to a method of trimming a voltage comprising: "receiving an input voltage to be trimmed; performing a constant load current and constant feedback impedance voltage trim process on said input voltage; and outputting a trimmed voltage from said input voltage."

Applicants respectfully submit that Jaussi does not teach or suggest, either expressly or inherently, either receiving an input voltage to be trimmed, or performing a constant load current and constant feedback impedance voltage trim process on said input voltage, or outputting a trimmed voltage from said

input voltage, as claimed. Rather, Jaussi discloses a current reference controlled by a control loop, see e.g., Fig 5, and col. 6 lines 28 - 32. Therefore, Figure 5 of Jaussi describes attempting to output a constant current at node 510, not a trimmed voltage. Jaussi discloses receiving an input voltage (Vref), but this input voltage is only used as an input to a comparator, not as an input voltage to be trimmed as in the claimed embodiment of the present invention. Additionally, since input voltage Vref is only used as an input to voltage comparator 304, a constant load current and constant feedback impedance voltage trim process is not performed on the input voltage as in the claimed embodiment of the present invention, see e.g., Figure 5 of Jaussi.

Further, according to Jaussi, deviations to the desired constant current are corrected via feedback loop utilizing voltage variations detected by voltage comparator 304, see e.g., Figure 3, Figure 5, col. 5 lines 14 - 31, and col. 3 lines 42 - 50 of Jaussi. This means that gate 510 in Figure 5 of Jaussi does not output a trimmed voltage from said input voltage, as claimed in the present invention, but rather outputs a current that generates a varying voltage (not a trimmed voltage) across an external resistor, see e.g., Figure 5 and Col. 5, lines 14 - 31 of Jaussi. Consequently, Jaussi does not anticipate or render obvious, the embodiment of the Applicants' invention as recited in Claim 8, and as such Claim 8 overcomes the rejection under 35 U.S.C. 102(e).

Claims 8 - 12 are rejected under 35 U.S.C. 102(e), as being anticipated by Burger, Jr. et al. U.S. Patent No. 6,275,090 (hereinafter Burger). Applicants have reviewed the cited portions of the reference, and submit that embodiments of the present invention as recited in Claims 8 - 12 are neither anticipated nor rendered obvious by the cited portions of Burger. The Examiner is respectfully directed to independent Claim 8 that has been presented above. Claims 9 - 12 depend from Claim 8 and recite further limitations of the claimed invention.

Applicants respectfully submit that the cited portions of Burger do not teach or suggest, either expressly or inherently, performing a constant load current and constant feedback impedance voltage trim process on said input voltage; and outputting a trimmed voltage from said input voltage, as claimed. Burger teaches receiving an input voltage (V_{BG}), see e.g., Figure 1 of Burger. However, Burger does not teach either performing a constant load current and constant feedback impedance voltage trim process on said input voltage, or outputting a trimmed voltage from said input voltage, as claimed. Instead, Burger teaches using the input voltage (V_{BG}) only as an input to a comparator, without performing any trimming on or feedback with V_{BG}. Further, Burger teaches away from the claimed embodiment of the present invention by teaching an output voltage at node 112 that is a binary high or low based on a comparison to the input voltage V_{BG} performed by comparator 110, rather than outputting a trimmed output voltage from said input voltage, as recited in the claimed invention, see e.g., Figure 1 and Figure 2 of Burger.

Consequently, Burger does not anticipate or render obvious, the embodiments of the Applicants' invention as recited in Claim 8, and as such Claim 8 overcomes the rejection under 35 U.S.C. 102(e). Accordingly, Applicants also respectfully submit that Burger fails to anticipate or render obvious the Applicants' invention as set forth in Claims 9 - 12 dependent on Claim 8; and that Claims 9 - 12 overcome the rejection under 35 U.S.C. 102(e) through dependency on an allowable base claim.

35 U.S.C. §103 Rejections

Claims 1 and 6 - 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikehashi, Japanese Patent No. JP 2000-049283 (hereinafter Ikehashi) in view of one of ordinary skill in the art. Applicants have reviewed the cited portion of the reference, and respectfully submit that the embodiments of the present invention as recited in Claims 1 and 6 - 8 are neither anticipated nor rendered obvious by the cited portion of Ikehashi in further view of one of ordinary skill in the art.

The Examiner is respectfully directed to independent Claim 1, which recites that an embodiment of the present invention is directed to a voltage trim circuit comprising:

> ...a voltage divider circuit coupled to said operational amplifier, said transistor and an output, wherein an output voltage is generated as a function of an adjustable divider ratio, and wherein a substantially constant feedback path is provided to said operational amplifier; and

a bias current circuit coupled to said voltage divider circuit and a second potential, wherein an adjustable resistive load is configurable to maintain a substantially constant load current through said transistor.

Claims 6 - 7 depend from independent Claim 1 and recite further limitations of the claimed invention. Independent Claim 8 contains some similar limitations to Claim 1 and was rejected with the same rationale as Claim 1.

Applicants respectfully submit that Ikehashi does not teach or suggest, either expressly or inherently, either a voltage divider circuit wherein an output voltage is generated as a function of an adjustable divider ratio, or a bias current circuit with an adjustable resistive load as in the claimed embodiment of the present invention. The circuit disclosed in Ikehashi teaches away from the present invention as claimed by teaching a non-adjustable voltage divider rather than an adjustable voltage divider as in the claimed embodiment of the present invention, see e.g., Ra and R1 of Figure 10 in Ikehashi. Further, since the output voltage (Vref) is taken from a fixed point above the divider network, it is not generated as a function of the voltage divider, as the output voltage is in the claimed embodiment of the present invention, see e.g. Figure 10 in Ikehashi.

Additionally, the circuit disclosed in the cited Ikehashi reference is silent with respect to a bias circuit with an adjustable resistive load configurable to maintain a substantially constant load current through said transistor, as claimed. The rejection cites that one of ordinary skill in the art would have modified the circuit of Ikehashi in such a manner as to select a value of Rb to be

changed proportional to the value of Vbg. In the event that Ikehashi is again used as a basis for rejection, Applicants request that the Examiner provide a complete translation of Ikehashi so that its teachings can be fully understood and appreciated by both the Examiner and the Applicants. At present, Applicants can find no motivation in the cited Ikehashi reference for making the modification to the circuit suggested by the Examiner, and invite the Examiner to identify such a motivation within the text. Applicants also respectfully point out that such a modification is inconsistent with the Examiner's inclusion of a portion of Rb (namely R1) as an element of a voltage divider.

Therefore, the embodiments of the Applicants' invention set forth in Claims 1 and 8 are neither anticipated nor rendered obvious by Ikehashi in view of one of ordinary skill in the art. Likewise, embodiments of the present invention as claimed in Claims 6 - 7, which depend from Claim 1, are neither anticipated nor rendered obvious by Ikehashi in view of one of ordinary skill in the art. Accordingly, the Applicants also respectfully submit that Claims 1 and 8 overcome the rejection under 35 U.S.C. 103(a), and that Claims 6 and 7, which depend from Claim 1, also overcome the rejection under 35 U.S.C. 103(a) through dependency on an allowable base claim.

Claims 2 - 3 and 9 - 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikehashi in view of Wu et al. U.S. Patent No. 6,542,026 (hereinafter Wu). Applicants have reviewed the cited portions of the references, and respectfully submit that the embodiments of the present invention as recited

in Claims 2 - 3 and 9 - 17 are neither anticipated nor rendered obvious by the cited portions of Ikehashi or Wu, either alone or in combination.

With respect to Claims 2 - 3 and 9 - 12 Applicants respectfully submit that Wu does not cure the deficiencies of Ikehashi as noted above with respect to Claims 1 and 8. Therefore, Applicants submit that Claims 2 - 3 which depend from Claim 1, and Claims 9 - 12 which depend from Claim 8, overcome the rejection under 35 U.S.C. 103(a) through dependency on allowable base claims.

Examiner is respectfully directed to independent Claim 13, which recites that an embodiment of the present invention is directed to a system of generating a desired output voltage from an input voltage utilizing a voltage trim circuit comprising: "... a bias current circuit coupled to said voltage divider circuit and for selectively adjusting a resistance to maintain a substantially constant load current over said range of input voltage levels," as claimed. Claims 14 - 17 depend from independent Claim 13 and recite further limitations of the claimed invention.

Applicants submit that Wu does not correct the previously noted deficiencies of Ikehashi. As noted above with respect to Claim 1, the circuit disclosed in the cited Ikehashi reference is silent with respect to a bias current circuit coupled to said voltage divider circuit and for selectively adjusting a resistance to maintain a substantially constant load current over said range of

input voltage levels, as claimed. The rejection cites that one of ordinary skill in the art would have modified the circuit of Ikehashi in such a manner as to select a value of Rb to be changed proportional to the value of Vbg. At present, Applicants can find no motivation in the cited Ikehashi reference for making the modification to the circuit suggested by the Examiner, and invite the Examiner to identify such a motivation within the text. Further, such a modification is inconsistent with the Examiner's inclusion of a portion of Rb (namely R1) as an element of a voltage divider.

Additionally, Applicants can find no motivation in the cited portions of Ikehashi for adding a second voltage divider circuit, such as the circuit from Wu, to the circuit of Ikehashi. It is conceivable that such a change could negate the functionality of the cited circuit of Ikehashi. See e.g., Figure 10 of Ikehashi. Because of this, if Ikehashi is continued to be used as a basis for rejection, Applicants once again request that the Examiner provide a complete translation of Ikehashi so that its teachings can be fully understood and appreciated by both the Examiner and the Applicants. Consequently, the embodiments of the Applicants' invention set forth in Claim 13 are neither anticipated nor rendered obvious by Ikehashi or Wu, either alone or in combination. Likewise, embodiments of the present invention as claimed in Claims 14 - 17, which depend from Claim 13, are neither anticipated nor rendered obvious by Ikehashi or Wu, either alone or in combination.

Therefore, the combination of Ikehashi and Wu does not anticipate or render obvious, the embodiments of the Applicants' invention as recited in Claim 13, and as such Claim 13 overcomes the rejection under 35 U.S.C. 103(a). Accordingly, the Applicants also respectfully submit that the combination of Ikehashi and Wu fails to anticipate or render obvious the Applicants' invention as set forth in Claims 14 - 17 dependent on Claim 13, and that Claims 14 – 17 overcome the rejection under 35 U.S.C. 103(a) through dependency on an allowable base claim.

Claims 4 - 5 and 18 - 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikehashi in view of Burger. Applicants have reviewed the cited portion of the references, and respectfully submit that the embodiments of the present invention as recited in Claims 4 - 5 and 18 - 20 are neither anticipated nor rendered obvious by the cited portions of Ikehashi or Burger, either alone or in combination.

Claims 4 – 5 depend from independent Claim 1. Claims 18 – 20 depend from independent Claim 13. The addition of the Burger reference does not cure the deficiencies in the Ikehashi reference, as noted above, in regard to Claims 1 and 13. Therefore, Applicants submit that Claims 4 - 5 which depend from Claim 1, and Claims 18 - 20 which depend from Claim 13, overcome the rejection under 35 U.S.C. 103(a) through dependency on allowable base claims.

SUMMARY

In view of the foregoing remarks, the Applicants respectfully submit that the pending claims in the instant patent application are in condition for allowance. The Applicants respectfully request reconsideration of the Application and allowance of the pending claims. If the Examiner determines the prompt allowance of these claims could be facilitated by a telephone conference, the Examiner is invited to contact the Applicant's designated representative at the below listed phone number.

Respectfully submitted,
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Dated: 21 June, 2005

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